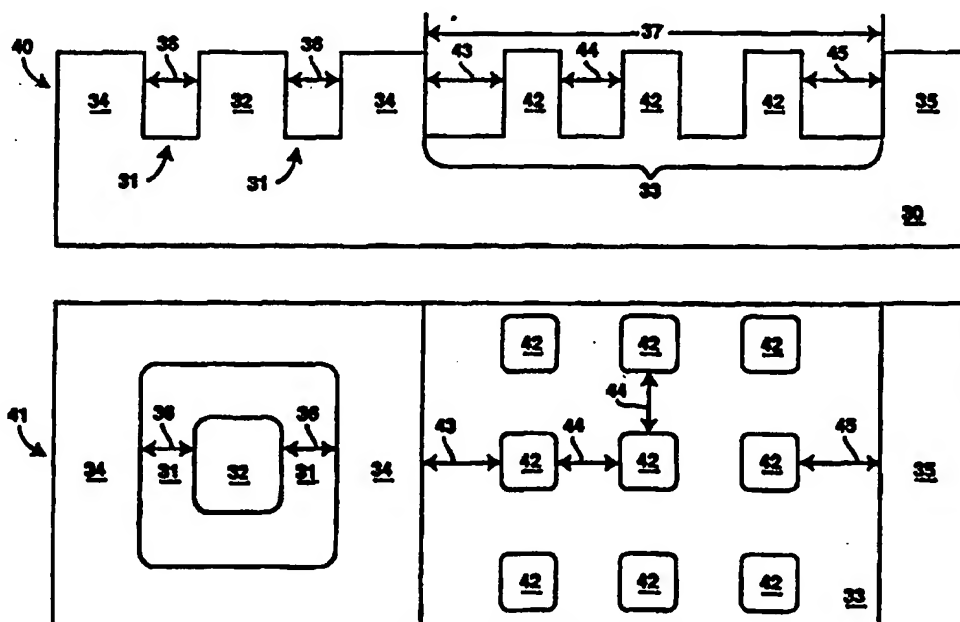


**PCT**WORLD INTELLECTUAL PROPERTY ORGANIZATION  
International Bureau

## INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

<b>(51) International Patent Classification <sup>5</sup>:</b> <b>H01L 23/053, 23/12, 23/48, 23/52, 21/76, 21/48</b>	<b>A1</b>	<b>(11) International Publication Number:</b> <b>WO 96/15552</b> <b>(43) International Publication Date:</b> 23 May 1996 (23.05.96)
<b>(21) International Application Number:</b> PCT/US95/14681 <b>(22) International Filing Date:</b> 13 November 1995 (13.11.95) <b>(30) Priority Data:</b> 08/337,000 10 November 1994 (10.11.94) US <b>(71) Applicant:</b> INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US). <b>(72) Inventors:</b> MOON, Peter, K.; 4901 S.W. 26th Drive, Portland, OR 97201 (US). SARANGI, Ananda, G.; 16795 S.W. Ivy Glenn Street, Beaverton, OR 97007 (US). DEETER, Timothy, L.; 3359 N.W. 125th Place, Portland, OR 97229 (US). <b>(74) Agents:</b> BEREZNAK, Bradley, J. et al.; Blakely, Sokoloff, Taylor & Zafman, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025-1026 (US).		<b>(81) Designated States:</b> AL, AM, AT, AT (Utility model), AU, BB, BG, BR, BY, CA, CH, CN, CZ, CZ (Utility model), DE, DE (Utility model), DK, DK (Utility model), EE, EE (Utility model), ES, FI, FI (Utility model), GB, GE, HU, IS, JP, KE, KG, KP, KR, KZ, LK, LR, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SK (Utility model), TJ, TM, TT, UA, UG, UZ, VN, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG), ARIPO patent (KE, LS, MW, SD, SZ, UG).  <b>Published</b> <i>With international search report.</i> <i>Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.</i>

**(54) Title:** FORMING A PLANAR SURFACE OVER A SUBSTRATE BY MODIFYING THE TOPOGRAPHY OF THE SUBSTRATE**(57) Abstract**

A method of forming a substantially planar surface over a trench isolation region (33) of a semiconductor substrate (30). Latent active regions (42) are formed within the trench isolation region (33). A dielectric layer (38) is then deposited over the surface of the semiconductor substrate (30). Then, the dielectric layer (38) is polished back to form a planar surface.

**FOR THE PURPOSES OF INFORMATION ONLY**

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AT	Austria	GB	United Kingdom	MR	Mauritania
AU	Australia	GE	Georgia	MW	Malawi
BB	Barbados	GN	Guinea	NE	Niger
BE	Belgium	GR	Greece	NL	Netherlands
BF	Burkina Faso	HU	Hungary	NO	Norway
BG	Bulgaria	IE	Ireland	NZ	New Zealand
BJ	Benin	IT	Italy	PL	Poland
BR	Brazil	JP	Japan	PT	Portugal
BY	Belarus	KE	Kenya	RO	Romania
CA	Canada	KG	Kyrgyzstan	RU	Russian Federation
CF	Central African Republic	KP	Democratic People's Republic of Korea	SD	Sudan
CG	Congo	KR	Republic of Korea	SE	Sweden
CH	Switzerland	KZ	Kazakhstan	SI	Slovenia
CI	Côte d'Ivoire	LJ	Liechtenstein	SK	Slovakia
CM	Cameroon	LK	Sri Lanka	SN	Senegal
CN	China	LU	Luxembourg	TD	Chad
CS	Czechoslovakia	LV	Latvia	TG	Togo
CZ	Czech Republic	MC	Monaco	TJ	Tajikistan
DE	Germany	MD	Republic of Moldova	TT	Trinidad and Tobago
DK	Denmark	MG	Madagascar	UA	Ukraine
ES	Spain	ML	Mali	US	United States of America
FI	Finland	MN	Mongolia	UZ	Uzbekistan
FR	France			VN	Viet Nam
GA	Gabon				

WO 96/15552

PCT/US95/14681

-1-

## **FORMING A PLANAR SURFACE OVER A SUBSTRATE BY MODIFYING THE TOPOGRAPHY OF THE SUBSTRATE**

### **FIELD OF THE INVENTION**

The present invention relates to semiconductor processing and more particularly to a method of forming a planar surface in a semiconductor device.

### **BACKGROUND OF INVENTION**

In order to increase the speed and functionality of electronic equipment such as, for example, home computers and other electronic consumer products, it is necessary to pack more transistors into the semiconductor devices contained within this electronic equipment. In addition to increasing the speed and functionality of electronic equipment, consumers demand that the equipment be miniaturized. To support the needs of the consumer, semiconductor device manufacturers have developed many techniques to reduce the size of transistors contained in semiconductor devices.

To reduce the size of transistors in a semiconductor device, it is necessary to minimize the line width of the polysilicon lines from which the transistors are formed. The width of these polysilicon lines is determined by a photolithography process. In the photolithography process, photographic techniques are used to transfer an image of the desired polysilicon pattern to the surface of a polysilicon layer within the semiconductor device. Then, after unneeded portions of the polysilicon layer are etched away, the image of the desired polysilicon pattern is manifested within the polysilicon material.

Because photo-optics are used in the photolithography process, photo-optic concerns such as resolution and depth of focus become important factors in the manufacture of semiconductor devices. For example, if the polysilicon layer is not entirely planar, then the polysilicon pattern image to be resolved on its surface will not be entirely in focus. This results in line width variation of the polysilicon lines formed from the image.

WO 96/15552

PCT/US95/14681

-2-

As polysilicon line widths are continually made smaller to accommodate the formation of proportionately smaller transistors, even minor variations in the line widths play an increasingly significant role in the operation of these transistors. Therefore, planarization becomes increasingly more important to reduce or eliminate polysilicon line width variations. By eliminating these variations, the resulting transistors operate more efficiently, reliably, and with greater speed. In addition, eliminating line width variations of the polysilicon allows circuit designers to more accurately characterize operation of the transistors, resulting in improved design efficiency.

Figures 1a-c illustrate a method of preparing a semiconductor substrate before deposition of the polysilicon layer from which transistors of the semiconductor device will be formed. For the foregoing reasons it is necessary that the surface of the semiconductor substrate be sufficiently planar before the polysilicon is deposited. In the first step illustrated in Figure 1a, trenches 11 and 13 are etched into semiconductor substrate 10. Trench regions 11 and 13 are referred to as *isolation regions* of the semiconductor device because these trenches serve to isolate electrically active components of the device from each other. For example, as illustrated both in cross section 20 and surface view 21 of semiconductor substrate 10, isolation region 11 is used to isolate region 12 from region 14 while isolation region 13 is used to isolate region 14 from region 15. Unetched regions 12, 14 and 15 are called *active regions* of the semiconductor device because electrically active components of the semiconductor device, such as transistors, are formed in these regions. Because isolation regions serve to isolate active regions from each other, transistors formed in active region 12 are allowed to operate independently of transistors formed in region 14. Likewise, transistors formed in region 14 are allowed to operate independently of transistors formed in region 15. Typically, isolation regions of a semiconductor device are of significantly varying widths. As illustrated, width 16 of isolation region 11 is much narrower than width 17 of isolation region 13.

WO 96/15552

PCT/US95/14681

-3-

After trenches are etched into the semiconductor substrate, a dielectric material is deposited as illustrated in Figure 1b. Dielectric layer 18 will coat the surface of semiconductor substrate 10, filling the trenches and covering the active regions. Note the significant dip in the surface of dielectric layer 18 above isolation region 13 caused by the large width of this trench. The non-planar topography of dielectric layer 18 in this region, along with the density differences between dielectric layer 18 and semiconductor substrate 10, results in the cross section illustrated in Figure 1c after a chemical mechanical polish is used to etch back dielectric layer 18.

As dielectric layer 18 is etched back to the surface of semiconductor substrate 10, the dip in the surface of dielectric layer 18 over isolation region 13 is propagated into the dip of dielectric layer 18 within isolation region 13 illustrated in Figure 1c. In addition, because dielectric layer 18 is a lower density than semiconductor substrate 10, it is polished at a faster rate than semiconductor substrate 10, which also contributes to this dip. In contrast, compare narrow trench isolation region 11. Narrow isolation regions such as this tend to exhibit more planarized topographies than wider isolation regions. One reason for this is because the chemical mechanical polish process used to etch back the dielectric layer is typically optimized to planarize narrow isolation regions rather than wide isolation regions. Also, the higher density of the semiconductor substrate material in this region improves the end-pointing of the chemical mechanical polish.

As a result, polysilicon lines formed on the surface of semiconductor substrate 10 in active regions 12 and 14 near isolation region 11 will lie substantially flat. Therefore, there will be no polysilicon line width variation in these regions. However, due to the abrupt topography in regions 19 at the upper corners of isolation region 13, the width of polysilicon lines overlying these regions will be altered. Consequently, transistors formed in active regions 14 and 15 will be impaired by polysilicon line width variations near the edges 19 of isolation region 13.

WO 96/15552

PCT/US95/14681

-4-

In addition to variation in polysilicon line width cause by the non-planarized surface of isolation region 13, the chemical mechanical polishing process used to etch back dielectric layer 18 causes damage to the semiconductor substrate near the edges 19 of the isolation region. Damage to the semiconductor substrate can impair the operation of transistors formed in the damaged active regions. Isolation region 11 does not suffer from semiconductor substrate damage because its planarized surface prevents such damage.

What is desired is a method for forming isolation regions in a semiconductor substrate wherein the surface of the substrate is substantially planarized. In this manner, problems associated with polysilicon line width variation and semiconductor substrate damage can be reduced or eliminated, resulting in more reliable and better performing semiconductor devices.

#### **SUMMARY OF THE PRESENT INVENTION**

A method of forming a substantially planar surface over a trench isolation region of a semiconductor substrate is described. Latent active regions are formed within the trench isolation region. A dielectric layer is then deposited over the surface of the semiconductor substrate. Then, the dielectric layer is polished back to form a planar surface.

#### **BRIEF DESCRIPTION OF THE DRAWINGS**

**Figure 1a** is an illustration of a cross sectional and surface view of a substrate after being etched.

**Figure 1b** is an illustration of a cross sectional view of the substrate of Figure 1a after a layer has been deposited.

**Figure 1c** is an illustration of a cross sectional view of the substrate of Figure 1b after the layer has been etched back.

WO 96/15552

PCT/US95/14681

-5-

**Figure 2a** is an illustration of a cross sectional and surface view of a substrate after being etched in accordance with the present invention.

**Figure 2b** is an illustration of a cross sectional view of the substrate of Figure 2a after a layer has been deposited.

**Figure 2c** is an illustration of a cross sectional view of the substrate of Figure 2b after the layer has been etched back.

**Figure 3a** is an illustration of a cross sectional view of a substrate after being etched.

**Figure 3b** is an illustration of a cross sectional view of the substrate of Figure 3a after a layer has been deposited.

**Figure 3c** is an illustration of a cross sectional view of the substrate of Figure 3b after the layer has been etched back.

#### DETAIL DESCRIPTION

A method for forming a planarized region during the manufacture of a semiconductor device is described. In the following description, numerous specific details such as relative feature dimensions, process sequences, material compositions, etc. are set forth in order to provide a more thorough understanding of the present invention. However, it will be obvious to one skilled in the art that the present invention may be practiced without employing these specific details. In other instances, well known processes and processing techniques have not been described in detail in order to avoid unnecessarily obscuring the present invention.

While diagrams representing various embodiments of the present invention are illustrated in Figures 2a-3c, these illustrations are not intended to limit the invention. The specific processes described herein are only meant to help clarify an understanding of the present invention

WO 96/15552

PCT/US95/14681

-6-

and to illustrate embodiments of how the present invention may be implemented in order to form a semiconductor device in accordance with the present invention. For the purposes of this discussion, a semiconductor substrate is a substrate comprising any material or materials used in the manufacture of a semiconductor device. A substrate is a structure on which or to which a processing step acts upon.

In accordance with the present invention, the design of isolation region 13 of figure 1a is modified to form isolation region 33 of Figure 2a. Within isolation region 33 of Figure 2a have been formed active regions 42. By modifying the design of the semiconductor device to photolithographically define active regions 42 prior to etching the trench regions of semiconductor substrate 30, active regions 42 are formed within what was formerly the large isolation region 13. Active regions 42 are formed in the same process step as active regions 32, 34, and 35 by blocking the anisotropic etch of trenches 31 and 33. Therefore, technically, only the remaining etched regions of trench isolation region 33 surrounding active regions 42 are still the true isolation regions within what would otherwise have been the wider trench isolation region of the device. However, active regions 42 are only active insofar as they are capable of sustaining transistors as are active regions 32, 34, and 35. But in accordance with the present invention, unlike active regions 32, 34, and 35, no transistors or any other semiconductor device components are formed in active regions 42. For this reason, active regions 42 are referred to as *latent* active regions.

Applicants have discovered that the addition of these latent active regions to trench isolation region 33, if properly located, does not significantly impact the isolation properties of the isolation region. Even though the effective area of isolation within trench isolation region 33 is diminished by the incorporation of latent active regions 42, trench isolation region 33 is still able to adequately isolate active region 34 from active region 35. As a result, the performance of isolation regions of semiconductor devices modified in accordance with the present invention is not significantly hindered. Therefore, since the size, shape,

WO 96/15552

PCT/US95/14681

-7-

and method of forming the isolation region need not be modified to preserve its isolation properties, the present invention may be easily incorporated into virtually any semiconductor device manufacturing method utilizing trench isolation regions.

By modifying the design of isolation region 33 to form active regions 42, the density of active regions within isolation region 33 is increased to more closely approximate the relative density of active regions elsewhere in the semiconductor device. Moreover, in accordance with the present invention, the sizes, shapes, and placement of latent active regions 42 within isolation region 33 are specifically selected to achieve a particular density of active regions within the trench. The latent active regions are designed such that the proportion of active region to isolation region within the trench is approximately equal to the proportion of active region to isolation region of the most densely compacted active and isolation region elsewhere in the semiconductor device. Then, by optimizing the chemical mechanical polishing process to form a planarized surface over a semiconductor substrate area having this particular proportion of active region to isolation region, the entire surface the semiconductor substrate will be planarized.

For example, assume that active regions 32 and 34 and isolation region 31 represent the most densely compacted active and isolation region on semiconductor substrate 30. If this were a microprocessor, this area of the semiconductor substrate may be a cell in the static random access memory (SRAM) portion of the semiconductor substrate where transistor density is at a maximum. As described above in conjunction with Figures 1a-c, this area is already adequately planarized by optimization of the chemical mechanical polish process. Therefore, by making isolation region 33 look more like the SRAM cell by introducing latent active regions 42 into the trench, the planarization of isolation region 33 will be similarly improved.

The locations of latent active regions 42 within isolation region 33 are chosen such that the functionality of the semiconductor device is not substantially altered by the presence of these active regions. In order to

WO 96/15552

PCT/US95/14681

-8-

determine the locations for latent active regions 42 within isolation region 33, an active region pattern comprising latent active regions 42 is defined wherein the sizes, shapes, and spacings of the latent active regions are selected in light of the considerations described above. Next, an isolation region is identified into which the active region pattern comprising latent active regions 42 will be placed. This is accomplished by locating an isolation region having dimensions large enough to accommodate active regions formed therein. For example, width 36 of isolation region 31 is too narrow for active regions to be formed therein, but width 37 of isolation region 33 is large enough to accommodate the small, latent active regions 42. Note that because the chemical mechanical polish process used to etch back the subsequently deposited dielectric layer is optimized to planarize the dielectric layer formed within a narrow isolation region, formation of active regions within isolation region 31 is unnecessary to improve planarization. However, absent latent active regions 42, wide isolation region 33 would otherwise exhibit planarity problems associated with etching back the subsequently deposited dielectric layer.

As described above, the dimensions of latent active regions 42, and the spacings 44 between them, are selected so as to raise the density of active regions within isolation region 33 to approach the density of active regions in an area elsewhere in the semiconductor device. However, the size and shape of latent active regions 42, and the spacings 44 between them, must also abide by the design rules of the process technology used to manufacture the semiconductor device. For example, minimum spacing and minimum dimension rules, which change according to the process technology employed, limit the spacings and dimensions of the latent active regions.

Once an isolation region has been identified for incorporation of latent active regions therein, the design of the semiconductor device is modified by filling the isolation region with the latent active region pattern. Then, latent active regions are selectively removed from the isolation region which may interfere with or otherwise alter the functionality of the device. For example, as illustrated in Figure 2a,

WO 96/15552

PCT/US95/14681

-9-

latent active region 42 must be placed a safe distance 43 from adjacent active region 34. In addition, latent active region 42 must also be placed a safe distance 45 from active region 35. The distances 43 and 45 are determined by the practitioner such that latent active regions 42 do not violate minimum dimension design rules or interfere with the operation of any semiconductor device components such as, for example, transistors within active regions 34 and 35 respectively.

To prevent the formation of any parasitic transistors in latent active regions 42, any latent active regions within isolation region 33 which would underlie a polysilicon line are removed. Otherwise, a breakdown of the gate oxide separating a polysilicon line from a latent active region in isolation region 33 could cause the gates of nearby transistors to be shorted to the substrate, destroying operation of the semiconductor device. In addition, latent active regions within isolation region 33 which would underlie a polysilicon line should be removed to avoid creating a parasitic conductive channel by polysilicon voltage induced inversion within the isolation region, thereby destroying the isolation properties of the region.

Finally, any latent active region 42 within isolation region 33 which would incorporate a well boundary of the well diffusion regions between active region 34 and 35 is removed. This is done to prevent problems such as shorting adjacent well regions to each other. For example, if the surface of a latent active region incorporating a well boundary is silicided, the silicide may electrically couple one well to the other at the surface of the latent active region. By shorting the wells together in this manner, operation of the semiconductor device is destroyed. In general, latent active regions 42 are not placed at any location within isolation region 33 that might detrimentally alter the functionality of the semiconductor device.

Alternatively, latent active regions may be designed into what would otherwise be a large isolation region of the semiconductor device by any one of a number of other methods suitable to the design methodologies which the practitioner employs. In addition, a practitioner may wish to, for example, avoid placing the latent active

WO 96/15552

PCT/US95/14681

-10-

regions within portions of the isolation region which underlie any polysilicon or other layer for some of the same concerns described above. Alternatively, the latent active regions within the isolation region may even be placed in a location within the isolation region which does alter the functionality of the semiconductor device. In such an embodiment, a practitioner may be willing to sacrifice some alteration of the functionality of the semiconductor device in exchange for gaining improved planarity. Finally, note that the specific minimum distances used to separate the latent active regions from each other within an isolation region and from other regions of the semiconductor device are heavily dependent upon the manufacturing technology employed to create the semiconductor device. As the dimensions of newer generations of manufacturing processes continue to shrink, so will these minimum distances of separation.

In accordance with the present invention, after isolation regions 31 and 33 are formed, a dielectric film 38 is deposited over the surface of semiconductor substrate 30 as illustrated in Figure 2b. Dielectric layer 38 comprises silicon dioxide (oxide) material and is deposited by a method which provides adequate filling of regions 31 and 33, plus enough additional oxide to form a substantial surface above semiconductor substrate 30 which can be etched back. Note that the dip in dielectric layer 18 over isolation region 13 illustrated in Figure 1b is not exhibited by the dielectric layer formed in accordance with the present invention as illustrated in Figure 2b. Active regions 42 within isolation region 33 have served to raise the surface of dielectric layer 38 within this region. Modifying the surface topography of dielectric 38 by modifying the underlying topography of semiconductor substrate 30 in this manner improves the planarizing effectiveness of the subsequent chemical mechanical polishing process.

Figure 2c illustrates the semiconductor substrate of Figure 2b after dielectric layer 38 has been chemically mechanically polished back to the surface of semiconductor substrate 30. Note the significant improvement in the surface planarity of the substrate illustrated in Figure 2c versus an analogous cross section of the substrate illustrated in

WO 96/15552

PCT/US95/14681

-11-

Figure 1c. The mechanisms by which the abrupt corner regions 19 were formed in isolation region 13 of Figure 1c have been counteracted by the presence of latent active regions 42 within isolation region 33 of Figure 2c. In particular, active regions 42 have raised the surface of dielectric layer 38 formed above isolation region 33, thereby eliminating any dips in the dielectric layer formed above this region. In addition, the presence of the higher density latent active regions 42 within isolation region 33 has prevented the chemical mechanical polish from over-etching the lower density oxide material of dielectric layer 38 within the isolation region. By forming substantially planar active and isolation regions from the semiconductor substrate, the subsequently formed polysilicon layer will also be planarized. Thus, the entire polysilicon layer surface will reside within a single focal plane of the photolithographic technology used to define the polysilicon lines, substantially reducing or eliminating polysilicon line width variation. As a result, the problems associated with polysilicon line width variation such as, for example, a loss in design efficiency, degraded transistor reliability, and slow transistor switching speeds, are significantly reduced or eliminated.

In an alternate embodiment, a single, large latent active region, rather than several smaller regions, is formed within the isolation region to improve the planarity at the surface of the isolation region. Alternatively, the shape of latent active regions designed into what would otherwise have been a large trench isolation region of the semiconductor device may be any regular or irregular polygon, rounded figure, or a combination of shapes. In addition, these latent active regions may form any regular or irregular pattern or sequence, or may even be randomly staggered. An important consideration is merely that a "high region" such as, for example, a latent active region in a trench, is formed in a portion of what would otherwise have been a larger "low region" of the substrate such as, for example, the trench isolation region itself.

In an embodiment of the present invention, the dielectric layer used to fill the trench isolation regions comprises a substantially

WO 96/15552

PCT/US95/14681

-12-

undoped oxide such as thermal oxide, borosilicate glass (BSG), phosphosilicate glass (PSG), borophosphosilicate glass (BPSG), silicon nitride, polysilicon, or any other material suitable for filling a trench isolation region. For example, in one embodiment the dielectric layer comprises a multi-layer stack wherein the etched trenched regions of a silicon substrate are oxidized to form a thin thermal oxide layer over which BPSG is deposited. Also, in an alternate embodiment of the present invention, the dielectric layer may be etched back to the surface of the semiconductor substrate using an alternate etching technique or combination of techniques including, for example, purely mechanical polishing, wet etching, or dry etching.

Finally, methods in accordance with the present invention may be implemented in a damascene process where high regions are designed and formed into what would otherwise have been a wide, low region of a dielectric substrate. A conductive material is then deposited over the surface of the dielectric substrate, substantially filling any gaps and coating the high and low regions of the substrate. Upon etching back the conductive material to the surface of the dielectric substrate using a chemical mechanical polish, the conductive material will become isolated within the low regions of the substrate, forming interconnect lines of the semiconductor device. In this embodiment, the presence of the high dielectric regions are used to prevent, for example, over-etching the surface of wide interconnect lines.

Techniques in accordance with the present invention may be implemented at any layer of the semiconductor device where a substantially planar surface is desired. For example, Figures 3a-c illustrate an embodiment of the present invention in which a planar surface is formed from an interlayer dielectric (ILD) material. In this embodiment, the ILD is used to physically and electrically isolate an entire layer of interconnects formed underneath the ILD from another layer of interconnects formed on the upper surface of the ILD. The ILD additionally serves to isolate one interconnect line from an adjacent interconnect line within the same layer of metal interconnects of the semiconductor device.

WO 96/15552

PCT/US95/14681

-13-

Figure 3a illustrates a cross section of a portion of a semiconductor device in which metal interconnect lines 61, necessary for proper operation of the semiconductor device, have been formed on top of substrate 60. Substrate 60 comprises the semiconductor materials used to form various components of the semiconductor device in lower layers. In accordance with the present invention, high regions 62 are designed into the wide low region between metal interconnect lines 61. High regions 62 are designed, patterned and formed from the same metal layer from which metal interconnect lines 61 are formed. High regions 62 are placed a sufficient distance from neighboring interconnect lines 61 so as not to alter the functionality of the semiconductor device. For example, high regions 62 must be located far enough away from interconnect lines 61 to not only satisfy minimum spacing design rules for the particular process technology employed but also to prevent detrimental cross-capacitive effects between adjacent metal lines. In addition, the effects high regions 62 have on the functionality of the semiconductor device are considered with respect to the placement of high regions 62 in the vicinity of interconnect lines in interconnect layers above and below the presently illustrated layer of the semiconductor device. Again, cross-capacitive effects are an important concern here as well.

Figure 3b illustrates the substrate of Figure 3a after a dielectric layer 63 has been deposited over the surface of the substrate. The dip 65 in the surface of dielectric layer 63 is illustrated as it would be formed in the absence of high regions 62. In the presence of high regions 62, however, the surface of dielectric layer 63 will take the profile illustrated by dotted line 64. Note how modifying the topography of the substrate underlying dielectric layer 63 by adding high regions 62 has eliminated the dip in the dielectric layer above this region.

Figure 3c illustrates the substrate of Figure 3b after a portion of dielectric layer 63 has been etched back using a chemical mechanical polish to form an ILD surface for the next layer of interconnects. In the absence of high regions 62, dip 65 in Figure 3b has caused the non-planar topography 67 illustrated in Figure 3c. The chemical mechanical

WO 96/15552

PCT/US95/14681

-14-

process used to form the final ILD surface will propagate dip 65 down into the final ILD surface forming dip 67. Dip 67 causes problems with the subsequently formed layer of interconnects, particularly in defining the line width of the interconnects using a photolithography process, as described above.

However, in the presence of high regions 62, the cross-sectional profile 64 of dielectric layer 63, as illustrated in Figure 3b, is more effectively planarized. The result of a chemical mechanical polish of dielectric layer 63 in the presence of high regions 62 is illustrated by dotted line 66 in Figure 3c. As shown, the presence of high regions 62 has improved the planarity of the surface of the ILD layer so that a subsequently formed metal interconnect layer exhibits reduced line width variation thereby aiding in semiconductor device miniaturization efforts. Note that in an alternate embodiment, similar results may be achieved by etching back dielectric layer 63 using a mechanical polish, wet etch, dry etch, or a combination of techniques.

Thus a method of forming a planar surface over a region of a substrate in a semiconductor device has been described. Planarity is achieved by modifying the topography of the underlying substrate.

WO 96/15552

PCT/US95/14681

-15-

**CLAIMS**

What is claimed is:

- 1) A method of forming a substantially planar surface over a trench isolation region of a semiconductor substrate in a semiconductor device, said method comprising the steps of:
  - a) forming a latent active region within said trench isolation region;
  - b) forming a dielectric layer over said semiconductor substrate; and
  - c) polishing said dielectric material to form said substantially planar surface.
- 2) The method of claim 1 wherein a plurality of latent active regions are formed within said trench isolation region.
- 3) The method of claim 1 wherein said dielectric layer comprises a material selected from the group consisting essentially of oxide, BSG, PSG, BPSG, nitride, and any combination thereof.
- 4) The method of claim 1 wherein said polishing of said dielectric material is accomplished using a chemical mechanical polishing technique.
- 5) The method of claim 1 wherein said latent active region is formed at a location within said trench isolation region determined by modifying a design of said trench isolation region of said semiconductor device.
- 6) The method of claim 2 wherein a design of said semiconductor device is modified such that said plurality of said latent active regions are formed at locations within said trench isolation region determined by designing a predetermined pattern of latent active regions within a design of said trench isolation region, and subsequently removing any of said designed latent active regions

WO 96/15552

PCT/US95/14681

-16-

which would substantially alter the functionality of said semiconductor device.

- 7) The method of claim 6 wherein said designed latent active regions are removed from locations within said design of said trench isolation region which are disposed within a predetermined proximity to borders of said design of said trench isolation region.
- 8) The method of claim 7 wherein said designed latent active regions are also removed from locations within said design of said trench isolation region which are disposed beneath a polysilicon feature.
- 9) The method of claim 6 wherein said predetermined pattern of said latent active regions is designed such that a density of said latent active regions in a given area of said pattern approaches a density of active regions within an area of equal size elsewhere in said semiconductor device.
- 10) The method of claim 1 wherein said semiconductor device comprises a plurality of trench isolation regions, each of said plurality of said trench isolation regions having a latent active region formed therein in substantially the same manner as said trench isolation region.
- 11) A method of forming a substantially planar surface over a trench isolation region of a semiconductor substrate in a semiconductor device, said method comprising the steps of:
  - a) forming a plurality of latent active regions within said trench isolation region by modifying a design of said trench isolation region of said semiconductor device;
  - b) forming a dielectric layer over said semiconductor substrate; and

WO 96/15552

PCT/US95/14681

-17-

- c) polishing said dielectric material to form said substantially planar surface.
- 12) The method of claim 11 wherein said dielectric layer comprises a material selected from the group consisting essentially of oxide, BSG, PSG, BPSG, nitride, and any combination thereof.
- 13) The method of claim 12 wherein said polishing of said dielectric material is accomplished using a chemical mechanical polishing technique.
- 14) The method of claim 11 wherein said plurality of said latent active regions are formed at locations within said trench isolation region determined by designing a predetermined pattern of latent active regions within a design of said trench isolation region, and subsequently removing any of said designed latent active regions which would substantially alter the functionality of said semiconductor device.
- 15) The method of claim 13 wherein said plurality of said latent active regions are formed at locations within said trench isolation region determined by designing a predetermined pattern of latent active regions within a design of said trench isolation region, and subsequently removing any of said designed latent active regions which would substantially alter the functionality of said semiconductor device.
- 16) The method of claim 14 wherein said designed latent active regions are removed from locations within said design of said trench isolation region which incorporate a well boundary within said trench isolation region.
- 17) The method of claim 15 wherein said designed latent active regions are removed from locations within said design of said

WO 96/15552

PCT/US95/14681

-18-

trench isolation region which are disposed beneath a polysilicon feature.

- 18) The method of claim 17 wherein said predetermined pattern of said latent active regions is designed such that a density of said latent active regions in a given area of said pattern approaches a density of active regions within an area of equal size elsewhere in said semiconductor device.
- 19) The method of claim 13 wherein said semiconductor device comprises a plurality of trench isolation regions, each of said plurality of said trench isolation regions having latent active regions formed therein in substantially the same manner as said trench isolation region.
- 20) A method of forming a substantially planar interlayer dielectric surface over a layer of interconnects in a semiconductor device, said method comprising the steps of:
  - a) forming a plurality of high regions between two interconnects in said layer of interconnects, said high regions being formed from the same layer from which said interconnects are formed;
  - b) forming a dielectric layer over said layer of interconnects; and
  - c) polishing said dielectric material to form said substantially planar surface.

WO 96/15552

PCT/US95/14681

1/5

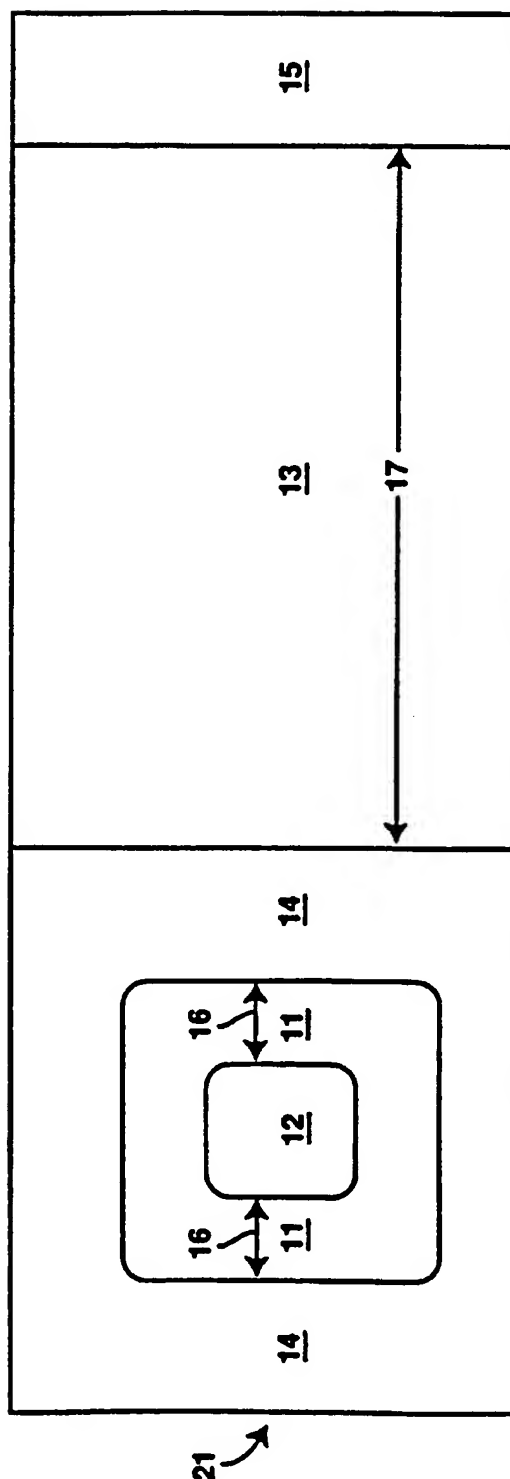
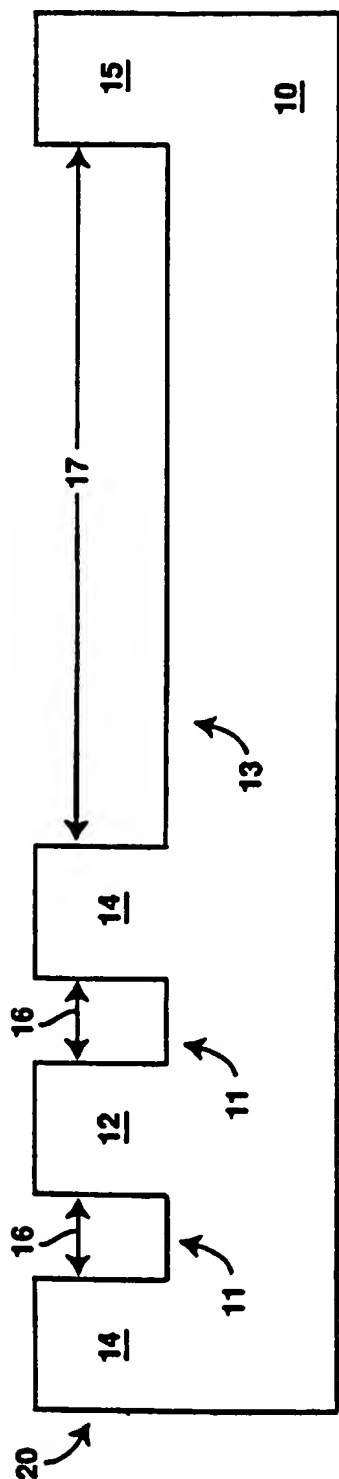
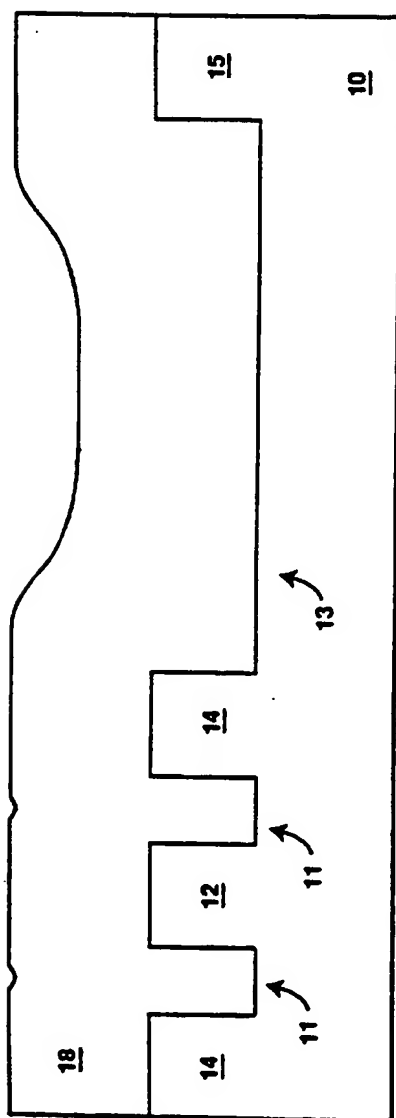


Figure 1a  
(Prior Art)

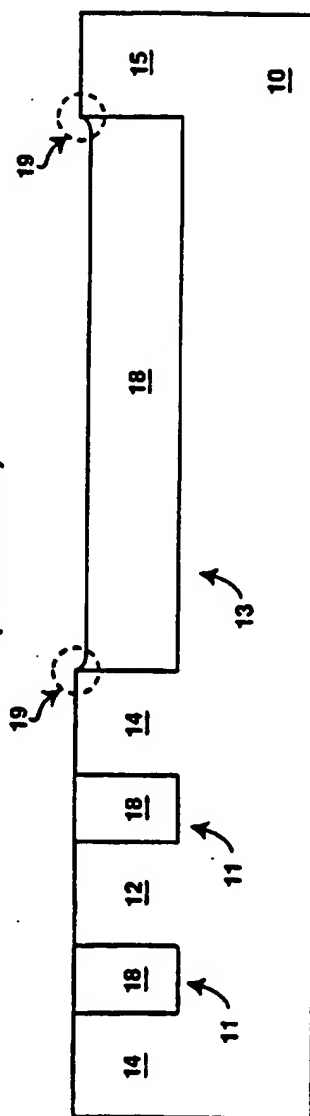
WO 96/15552

PCT/US95/14681

2/5



**Figure 1b**  
(Prior Art)



**Figure 1c**  
(Prior Art)

WO 96/15552

PCT/US95/14681

3/5

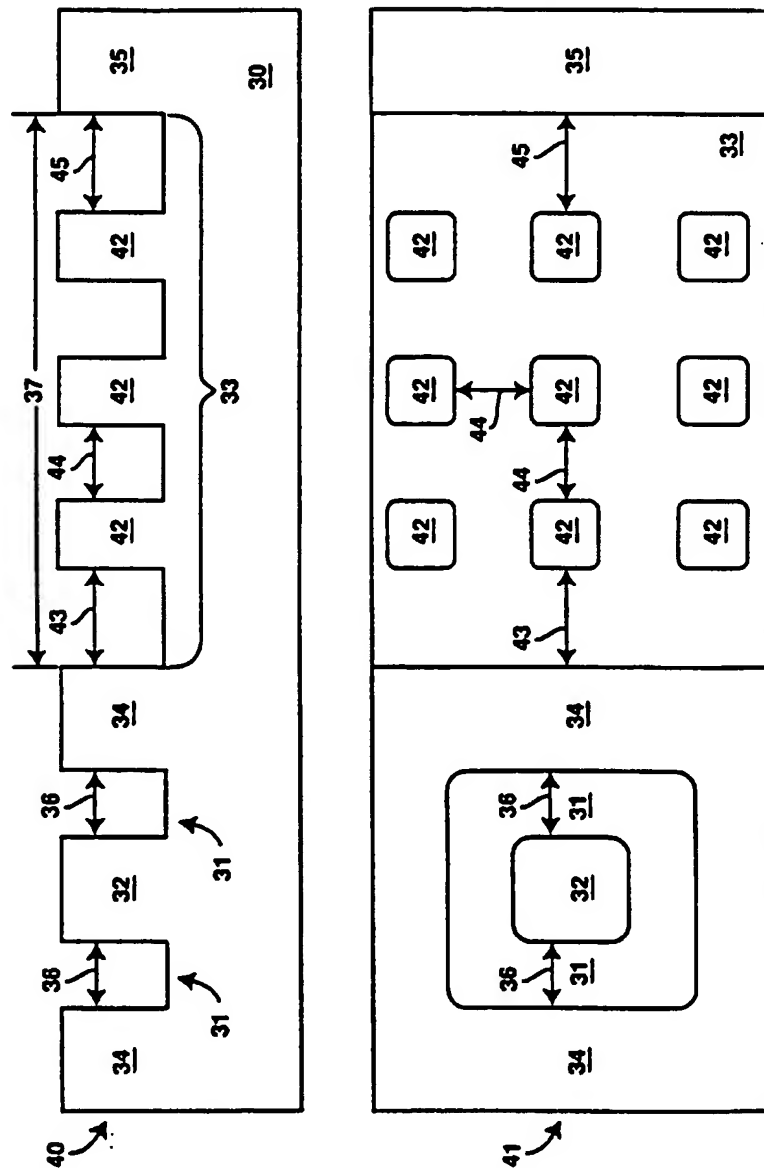


Figure 2a

WO 96/15552

PCT/US95/14681

4/5

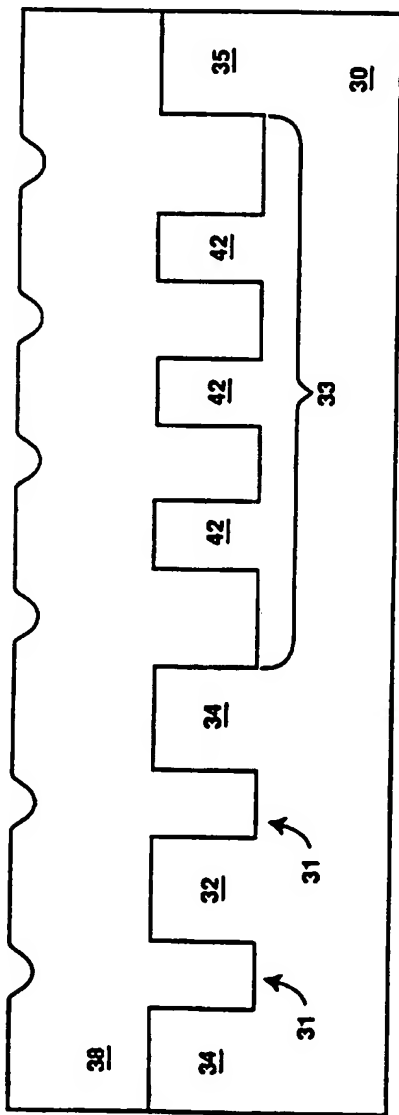


Figure 2b

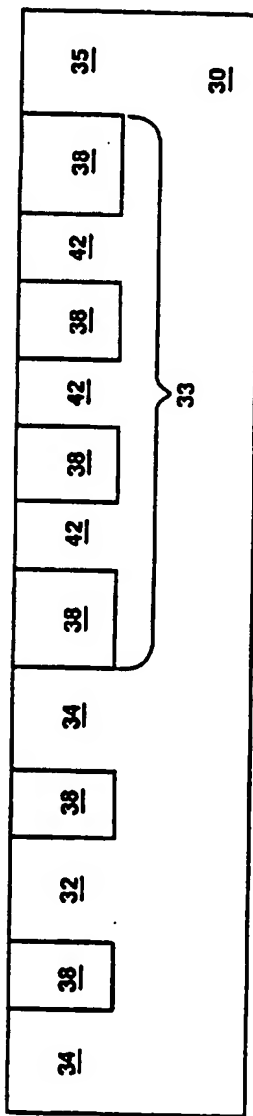


Figure 2c

WO 96/15552

PCT/US95/14681

5/5

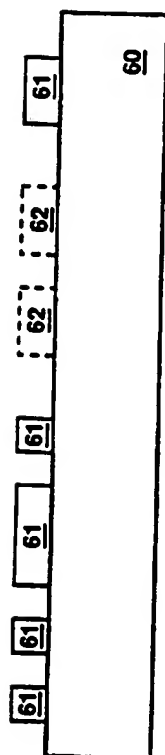


Figure 3a

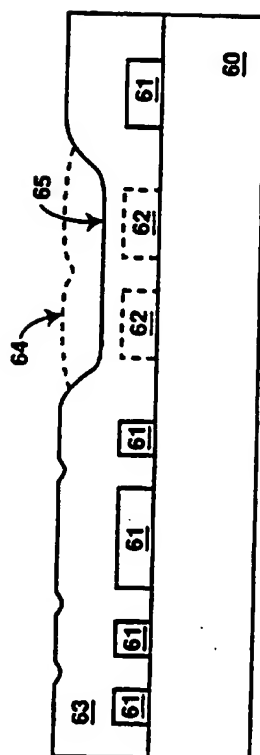


Figure 3b

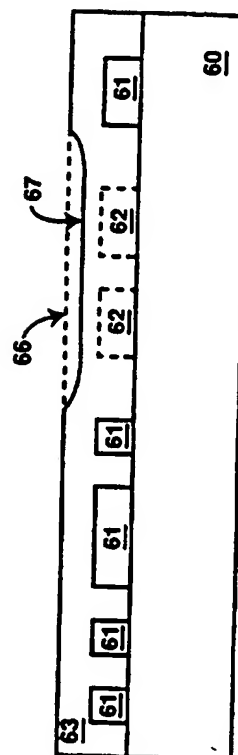


Figure 3c

## INTERNATIONAL SEARCH REPORT

International application No.  
PCT/US95/14681

**A. CLASSIFICATION OF SUBJECT MATTER**

IPC(5) : H01L 23/053, 23/12, 23/48, 23/52, 21/76, 21/48

US CL : 257/700, 752, 758, 773; 437/63, 64, 67, 72, 187, 195

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 257/700, 752, 758, 773; 437/63, 64, 67, 72, 187, 195

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS

Search terms: dummy, isolation, trench, chem-mech polishing, interconnection

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP, A, 60-15944 (Hitachi Seisakusho K.K.) 26 January 1985, English Abstract, Figs. 1-6.	1-19.
Y	JP, A, 59-186342 (Matsushita Denki Sangyo K.K.) 23 October 1984, Figs. 4(a)-(c) and page 226, last column.	1-19.
Y	US, A, 5,229,316 (Lee et al) 20 July 1993, col. 5, lines 3-18.	1-19.
X	US, A, 5,265,378 (Rostoker) 30 November 1993, col. 5, lines 10-64, Fig. 1.	20.
Y	JP, A, 63-240045 (Matsushita Electric Co., Ltd.) 5 October 1988, Abstract and Figs. 1-4.	20.



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A" document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"B" earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L" document which may throw doubt on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"A"	document member of the same patent family
"O" document referring to an oral disclosure, use, exhibition or other means		
"P" document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search

21 FEBRUARY 1996

Date of mailing of the international search report

14 MAR 1996

Name and mailing address of the ISA/US  
Commissioner of Patents and Trademarks  
Box PCT  
Washington, D.C. 20231

Facsimile No. (703) 305-3230

Authorized officer

TRUNG DANG

Telephone No. (703) 308-2548

## INTERNATIONAL SEARCH REPORT

International application No.  
PCT/US95/14681

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US, A, 5,225,358 (Pasch) 6 July 1993, col. 4, lines 18-48.	20.